

# Claims

- [c1] 1.A method for implementing a wiring translation in chip carrier module between corresponding points in a first grid and a second grid, the points in the first grid defining a first plane and the points in the second grid defining a second plane, the second plane lying substantially parallel to the first plane, the method comprising:  
connecting the first grid to a first translation layer within the module, said first translation layer translating the points in the first grid in a first direction; and  
connecting a second translation layer between said first translation layer and the second grid, said second translation layer translating the points in the first grid in a second direction, said second direction being orthogonal to said first direction.
- [c2] 2.The method of claim 1, wherein:  
said first translation layer is configured to include a first plurality of signal interconnects, said first plurality of signal interconnects each having a jog line elongated along said x-axis direction; and  
said second translation layer is configured to include a second plurality of signal interconnects, said second

plurality of signal interconnects each having a jog line elongated along said y-axis direction.

[c3] 3.The method of claim 2, wherein:  
each of said jog lines in said first plurality of signal interconnects is disposed between an upper via contact and a lower via contact in said first translation layer; and  
each of said jog lines in said second plurality of signal interconnects is disposed between an upper via contact and a lower via contact in said second translation layer.

[c4] 4.The method of claim 3, wherein:  
each individual upper via contact in said first translation layer is in electrical communication with a corresponding point in the first grid;  
each individual lower via contact in said first translation layer is in electrical communication with a corresponding upper via contact in said second translation layer; and  
each individual lower via contact in said second translation layer is in electrical communication with a corresponding point in the second grid;  
signal via in said first plurality of signal vias are in electrical contact with corresponding individual signal vias in said second plurality of signal vias.

[c5] 5.The method of claim 4, further comprising:  
configuring a first plurality of power busses in said first

translation layer, disposed along said x-axis direction;  
and  
configuring a second plurality of power busses in said  
second translation layer, disposed in said y-axis direc-  
tion.

- [c6] 6. The method of claim 1, wherein:  
said first grid comprises a C4 grid; and  
said second grid comprises a logic service terminal (LST)  
grid.